REMARKS

Upon entry of this amendment, claims 1-7, 10-13, 16-18, 21-25, 28 and 29 are all the claims pending in the application. Claims 8, 9, 14, 15, 19, 20, 26 and 27 are canceled by this Amendment.

Applicant thanks the Examiner for approving the substitute drawings filed on December 23, 2002.

I. Information Disclosure Statement

The Examiner has not initialed references 5-8 listed on form PTO-1449 submitted with the Information Disclosure Statement of October 26, 1999. These references are considered general background material, and thus, their English Abstracts were submitted with the Amendment filed December 23, 2002. Applicant requested that the Examiner initial references 5-8 listed on form PTO-1449 and re-submit initialed form PTO-1449.

In the Final Office Action, the Examiner states that the "information disclosure statement filed 12/23/02 fails to comply with 37 CFR 1.98(a), which requires a list of all patents, publications, or other information submitted for consideration by the Office." Applicant notes that an information disclosure statement was not filed on 12/23/02. Rather, Applicant submitted English Abstracts for references 5-8 submitted with the Information Disclosure Statement filed October 26, 1999. These references were listed in a foreign search report and are considered general background material only.

The Examiner requests that a new form PTO-1449 be submitted. For the Examiner's convenience, a clean form PTO-1449 is submitted herewith, listing references 5-8 of the Information Disclosure Statement filed October 26, 1999. Accordingly, Applicant respectfully requests that the Examiner initial the references listed on form PTO-1449 and submit initialed Form PTO-1449 with the next Office paper.

II. Claim Rejections under 35 U.S.C. § 102(b)

Claims 1-29 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Watanabe et al.(U.S. Patent No. 5,590,306). Applicant respectfully traverses this rejection on the following basis.

Claim 1, as amended, defines a novel combination of elements which form a computer having unique rewriting capabilities. Included among the features of this new computer is a controller which determines if a rewriting processing was performed without interruption by comparing a value read from a flag area to an expected flag value, whereby if the controller determines that the rewriting processing was interrupted, resuming the rewriting processing at the stage at which the rewriting processing was interrupted. Applicant submits that the claimed combination, including at least this feature, is neither disclosed nor suggested by Watanabe.

Watanabe discloses data packets having a read protect bit which is able to hold values of either "0" or "1" (see column 11, lines 51-54). When a writing process begins, a read protect bit is set to "1" (see column 16, lines 24-29). If the writing process is successful, the read protect bit is changed from "1" to "0" (see column 16, lines 29-32). However, if an error occurs during writing

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(e.g., the memory card is ejected during the writing operation), the read protect bit retains a value

of "1" because the writing process never completed (see column 16, lines 32-36). Thus, the

system is able to determine which packets did not undergo a successful writing operation by

monitoring which data packets have a read protect bit value of "1" (see column 16, lines 36-38).

When a data packet having a read protect bit value of "1" is detected, all of the packet data

is saved and the memory card is subsequently initialized (i.e., erased)(see column 12, lines 17-23

and column 16, lines 45-52). Only packets having a read protect bit value of "0", indicating normal

recording, are recorded onto the memory card (see column 12, lines 24-27 and column 16, lines

20-24 and lines 49-54). The defective data packets (i.e., having a read protect bit value of "1") are

erased during the initialization process and are not recorded onto the memory card (see column 17,

lines 1-4).

The Examiner points to columns 4 and 5 and column 14, lines 1-32 of Watanabe for

disclosing the feature of determining if a rewriting processing was performed without interruption

by comparing a value read from a flag area to an expected flag value, whereby if the controller

determines that the rewriting processing was interrupted, resuming the rewriting processing at the

stage at which the rewriting processing was interrupted. Applicant respectfully disagrees.

As explained above, Watanabe discloses a system which is able to determine if a rewriting

process was performed without interruption by comparing a bit value of a data packet to an

expected bit value. If the system determines that the rewriting process had an interruption,

however, the system does not resume the rewriting process at the stage where the interruption

occurred. Rather, the data packets that were subject to the interruption are simply erased, thereby freeing up storage capacity on the memory card (see column 16, lines 62-68).

The section referenced by the Examiner discloses an output operation being resumed upon the changing of a busy signal to a ready signal, but this section does not relate whatsoever to determining if a rewriting process was performed without interruption by comparing flag values. That is, while Watanabe is capable of making a determination as to whether a rewriting process has been interrupted by comparing bit values, Watanabe does not resume the rewriting process at the stage of interruption after this determination has been made, as is required by amended claim 1.

Therefore, as Watanabe fails to disclose or suggest all of the features of claim 1, Applicant respectfully requests that the Examiner reconsider and withdraw the rejection. If the Examiner persists in this rejection, Applicant respectfully requests that the Examiner particularly point out the passages in Watanabe which disclose the feature of "determining if a rewriting processing was performed without interruption by comparing a value read from a flag area to an expected flag value, whereby if the controller determines that the rewriting processing was interrupted, resuming the rewriting processing at the stage at which the rewriting processing was interrupted."

Claims 2 and 10-13 depend from claim 1 and therefore incorporate all of the limitations thereof. Accordingly, Applicant submits that these claims are patentable at least by virtue of their dependency.

Regarding independent claims 3, 4 and 7, Applicant submits that these claims are patentable for at least the same reasons as discussed above with respect to claim 1. Namely, Watanabe fails to disclose or suggest the feature of "determining if a rewriting processing was

performed without interruption by comparing a value read from a flag area to an expected flag value, whereby if the controller determines that the rewriting processing was interrupted, resuming the rewriting processing at the stage at which the rewriting processing was interrupted."

Claims 5, 16-18 and 24 depend from claim 1, claims 6, 21-23 and 25 depend from claim 4, and claims 28 and 29 depend from claim 7. Applicant submits that these claims are patentable at least by virtue of their dependency, and therefore, respectfully requests that the rejection be reconsidered and withdrawn.

III. Claim Rejections under 35 U.S.C. § 103(a)

Claims 2, 5, 6, 13, 24 and 25 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Watanabe et al. in view of Sukegawa et al. (U.S. Patent No. 5,603,001). Applicants respectfully traverse this rejection on the following basis.

Claims 2 and 13 depend from claim 1; claim 5 depends from claim 3; and claim 6 depends from claim 4. Applicant submits that Sukegawa fails to cure the deficient teachings of Watanabe with respect to independent claims 1, 3 and 4. Therefore, Applicant submits that claim 2, 5, 6, 13, 24 and 25 are patentable at least by virtue of its dependency and respectfully request that the rejection be reconsidered and withdrawn.

IV. Conclusion

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the

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Examiner feels may be best resolved through a personal or telephone interview, the Examiner is

kindly requested to contact the undersigned at the telephone number listed below.

Applicants hereby petition for any extension of time which may be required to maintain the

pendency of this case, and any required fee, except for the Issue Fee, for such extension is to be

charged to Deposit Account No. 19-4880.

Respectfully submitted,

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WASHINGTON OFFICE

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PATENT TRADEMARK OFFICE

Date: April 7, 2003

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<u>APPENDIX</u>

<u>VERSION WITH MARKINGS TO SHOW CHANGES MADE</u>

<u>IN THE CLAIMS</u>:

Claims 8, 9, 14, 15, 19, 20, 26 and 27 are canceled.

The claims are amended as follows:

1. (Twice Amended) A computer provided with a memory and having a self-programming function of rewriting a program stored in said memory, comprising:

a rewrite program area for storing a program for a rewriting processing procedure for said memory; and

a controller for forming a plurality of flag areas locally in said memory when the rewriting program is written into said memory, performing determination of completion of one or more stages of rewriting processing and recording results of the determination into the respective flag areas,

wherein the controller further determines if the rewriting processing was performed without interruption by comparing a value read from a flag area to an expected flag value, whereby if the controller determines that the rewriting processing was interrupted, resuming the rewriting processing at the stage at which the rewriting processing was interrupted.

3. (Twice Amended) A computer provided with a memory and having a self-programming function of rewriting a program stored in said memory, comprising:

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a rewrite program area for storing a program for a rewriting processing procedure for said

memory;

rewriting means for forming a plurality of flag areas locally in said memory when the

rewriting program is written into said memory; and

a controller for performing determination of completion of one or more stages of rewriting

processing and recording results of the determination into the respective flag areas through said

rewriting means,

wherein the controller further determines if the rewriting processing was performed

without interruption by comparing a value read from a flag area to an expected flag value, whereby

if the controller determines that the rewriting processing was interrupted, resuming the rewriting

processing at the stage at which the rewriting processing was interrupted.

4. (Twice Amended) A computer provided with a memory and having a self-programming

function of rewriting a program stored in said memory, comprising:

a rewrite program area for storing a program for a rewriting processing procedure for said

memory;

rewriting means for forming a plurality of flag areas locally in said memory when the

rewriting program is written into said memory;

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a controller for performing determination of completion of one or more stages of rewriting

processing and recording results of the determination into the respective flag areas through said

rewriting means; and

flag state notification means for comparing, when power supply is made available after the

rewriting is completed, values read out from said flag areas with expected values for said flag

areas stored in advance and notifying said controller of results of the comparison,

wherein the controller determines if the rewriting processing was performed without

interruption based on the results of the flag state notification means, whereby if the controller

determines that the rewriting processing was interrupted, resuming the rewriting processing at the

stage at which the rewriting processing was interrupted.

7. (Twice Amended) A method of storing a program into a memory of a computer

provided with said memory and having a self-programming function of rewriting the program

stored in said memory, wherein

a plurality of flag areas are formed locally in said memory when a rewriting program is

written into said memory, and determination of completion of one or more stages of rewriting

processing is performed, whereafter results of the determination are recorded into the respective

flag areas,

wherein the method further determines if the rewriting processing was performed without

interruption by comparing a value read from a flag area to an expected flag value, whereby if a

controller determines that the rewriting processing was interrupted, resuming the rewriting

processing at the stage at which the rewriting processing was interrupted.